**Amendments to the Claims:**

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Previously Presented) A coprocessor to a main processor having an execution speed greater than that of said processor, the coprocessor comprising a two-dimensional array of processing cells and being communicatively connected to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

2. (Previously Presented) The coprocessor of claim 1, wherein the array comprises a systolic processing array.

3. (Previously Presented) The coprocessor of claim 1, wherein the paths are connected one-to-one with said respective cells.

4. (Previously Presented) The coprocessor of claim 1, wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths.

5. (Previously Presented) The coprocessor of claim 1, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

6. (Previously Presented) A coprocessing system including the coprocessor, interface module and main processor of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection.

7. (Previously Presented) The coprocessor of claim 1, including an array processor that comprises said two-dimensional array.

8. (Previously Presented) An integrated circuit comprising the coprocessor of claim 1.

9-10. (Canceled)

11. (Previously Presented) The coprocessor of claim 1, wherein said processor comprises a digital signal processor.

12. (Previously Presented) The coprocessor of claim 1, wherein said processor comprises a general purpose processor.

13. (Previously Presented) A functional unit having two-dimensional array of processing cells and serving as a component of a main processor, the unit having a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

14. (Previously Presented) The unit of claim 13, wherein said processor comprises a very long instruction word (VLIW) processor.

15. (Previously Presented) The unit of claim 13, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose

row is the same and whose column is immediately adjacent.

16. (Previously Presented) The unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells.

17. (Previously Presented) A system including the processor of claim 16, and an array program generator for generating array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

18. (Previously Presented) The system of claim 17, further including a compiler configured for receiving, in response to said program updating, data representative of input and output timing for said unit and further configured for compiling an instruction based on said data.

19. (Canceled)

20. (Previously Presented) A method for interfacing a coprocessor to a main processor, comprising the steps of:

configuring the coprocessor to compromise a two-dimensional array of processing cells and to have an execution speed greater than that of said processor; and

communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

21. (New) The coprocessor of claim 1, wherein the array is rectangular,

wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array, and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

22. (New) The coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

23. (New) The coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array.

**Amendments to the Drawing Figures:**

The attached drawing sheet includes proposed changes to FIG. 2 and replaces the original sheets including FIG. 2

Attachment: Replacement Sheet